

# Quantum C100, a Wafer Scale CMOS Detector Optimised for 100 keV Cryo-Electron Microscopy

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## Abstract

Wafer scale CMOS image sensors are no longer a rarity thanks to the adoption and improvement of stitched manufacturing techniques. In this paper, in fact, we do not intend to focus on the sensor area, which is dictated by the application needs. What we want to showcase are the sensor performance relatively to the technology node used and its importance in the field the sensor has been designed for, cryo-electron microscopy (cryo-EM) at 100keV.

## Introduction

The success of CMOS image sensors for scientific applications like cryo-electron microscopy (cryo-EM) is demonstrated by the exponential growth of the cryo-EM field in the past years and confirmed by the number of entries in the world Protein Database System.

Recent publications<sup>1</sup> suggest reducing the operating voltage from 300keV to 100keV reduces sample damage and simultaneously allows for 25% more structural information<sup>1</sup>.

Optimal detection of 100keV electrons mean larger pixels and non-thinned sensors compared to 300keV. Thanks to the widespread availability of techniques like stitching, manufacturing wafer scale sensors on 8” or 12” platform is no longer limited to niche, low volumes applications<sup>2,3</sup>.

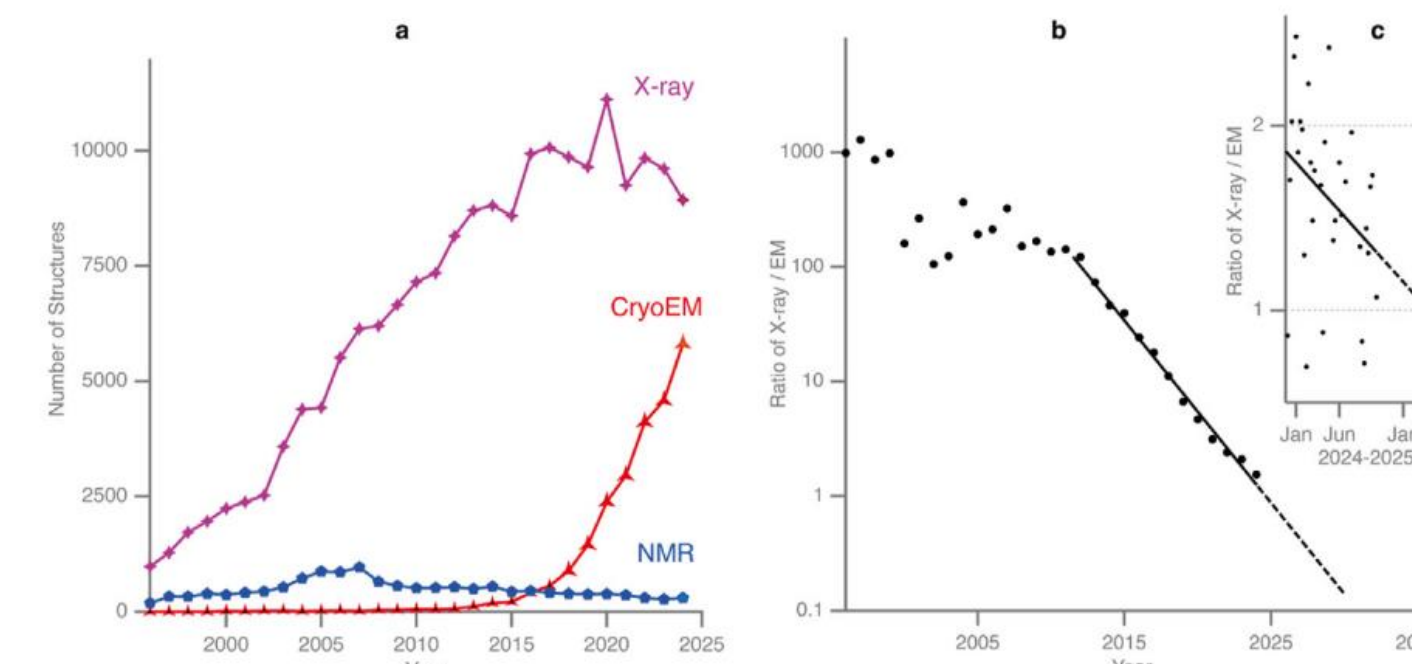


Figure 3 – X-rays vs. cryo-EM entries

Specification	Target
Sensor format	2048 x 2048
Pixel pitch	54 x 54 $\mu\text{m}$
Frame rate	2000 fps      2500 fps
Bit depth	12 bits      10 bits
Noise	52e- to 89e- rms, depending on gain
Full Well	6.1ke- to 30 ke-, depending on gain
Operation mode	Rolling shutter
Readout mode	Continuous
Readout type	Analogue CML lines
Sensor size	200 mm wafer-scale sensor
Manufacturing process	TowerJazz 180 nm CIS process
Sensitive area	104 $\text{cm}^2$
Radiation hard	YES
Back-thinning	NO
Dark pixels	Only on left and right sides of the pixel array

Figure 2 – C100 performance table

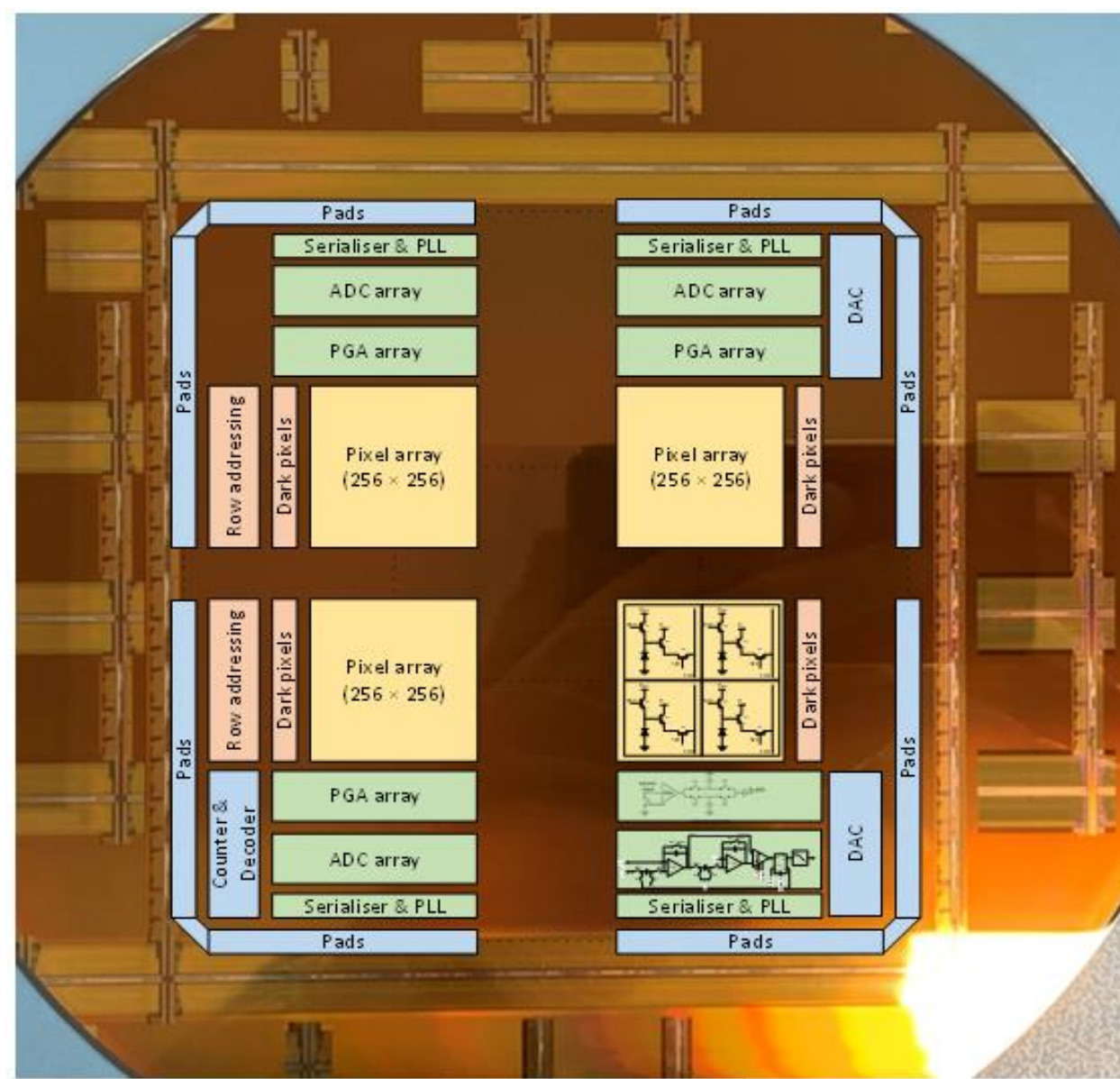


Figure 1 – C100 sensor floor plan

## Sensor Architecture

Quantum C100 is based on a rad-hard 3T pixel with rolling shutter readout and digital output. The relatively high frame rate has been achieved by reading out 8 rows at the same time.

The analogue pixel value is digitised on-chip using 16,384 second order, column parallel sigma-delta ADCs, chosen for its resilience over large mismatch-induced spread of the analogue stages<sup>4</sup>.

The sensor output data rate is ~100Gb/s. Handling such rate with LVDS lines will present integration challenges, which we have overcome by designing high speed output stages (up to 5Gb/s). Quantum C100 is equipped with 34 high speed output lines, operating at 4.3Gb/s with a XILINX AURORA® protocol<sup>5</sup>.

At full resolution the sensor achieves frame rates of 2,000 to 2,500fps with a 10 or 12 bit pixel depth, but can be operated up to 5,200fps changing the bit depth.

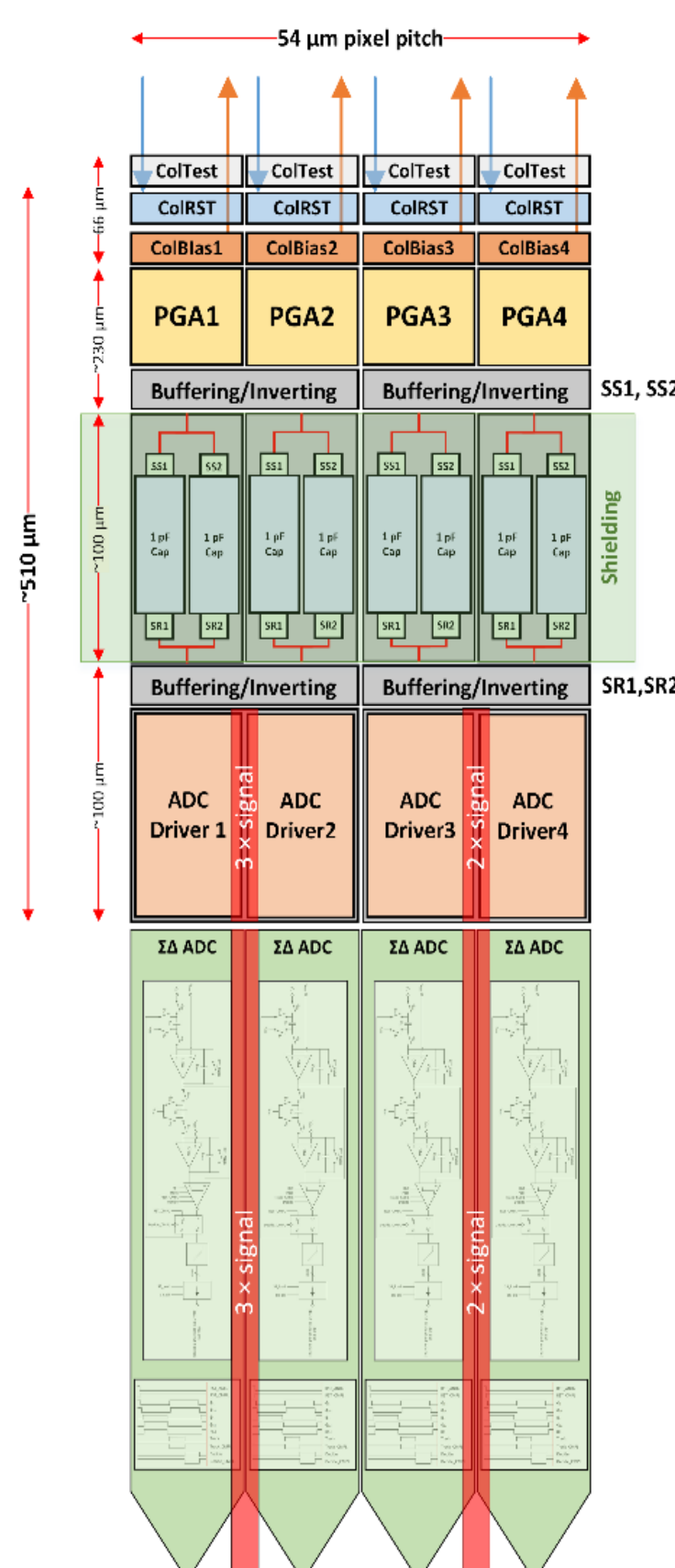


Figure 4 – C100 Column architecture

## Results

The performance of the wafer scale sensor are in line with simulated values and with the results obtained from a previous test structure. Thanks to a digitally programmable stage the gain be varied from 16  $\mu\text{V/e-}$  and 90  $\mu\text{V/e-}$ . Measured noise ranges from 52 e- rms to 89 e- rms depending on gain.

Full well with lower gain is ~30 ke- while it drops to 6.1ke- with the highest gain

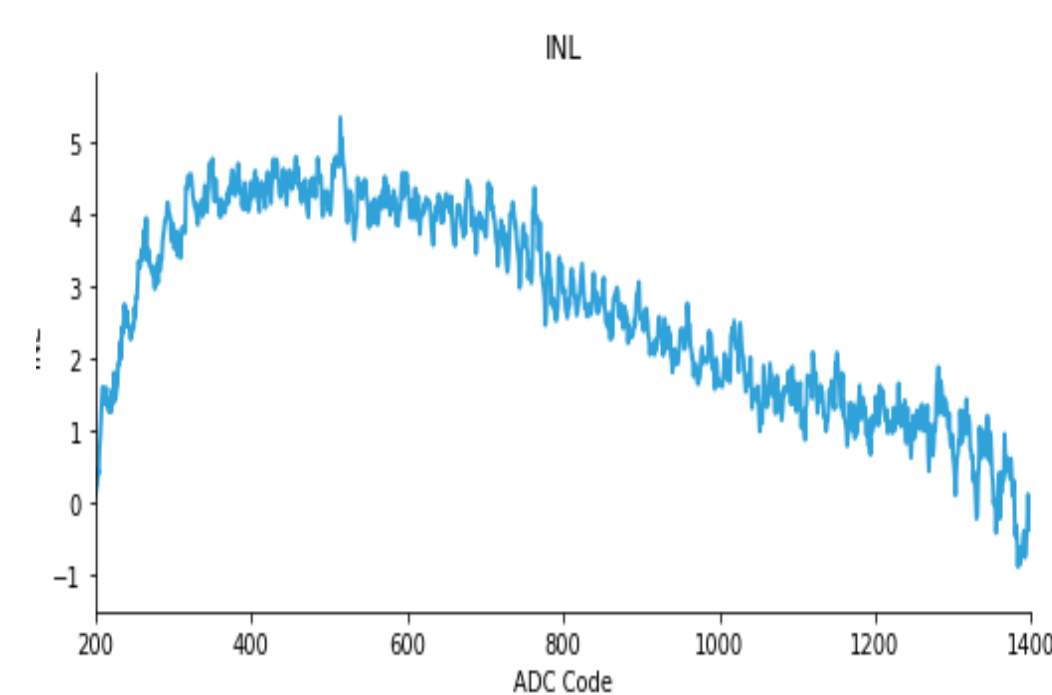


Figure 5 – Typical ADC INL

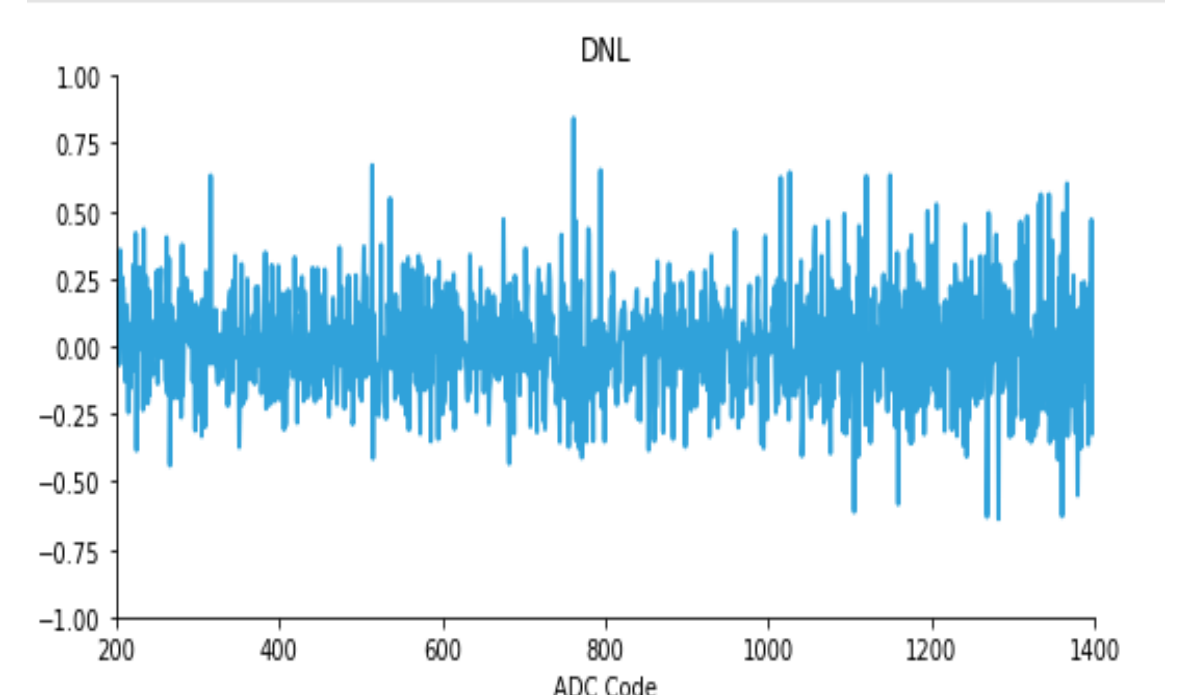


Figure 6 – Typical ADC DNL

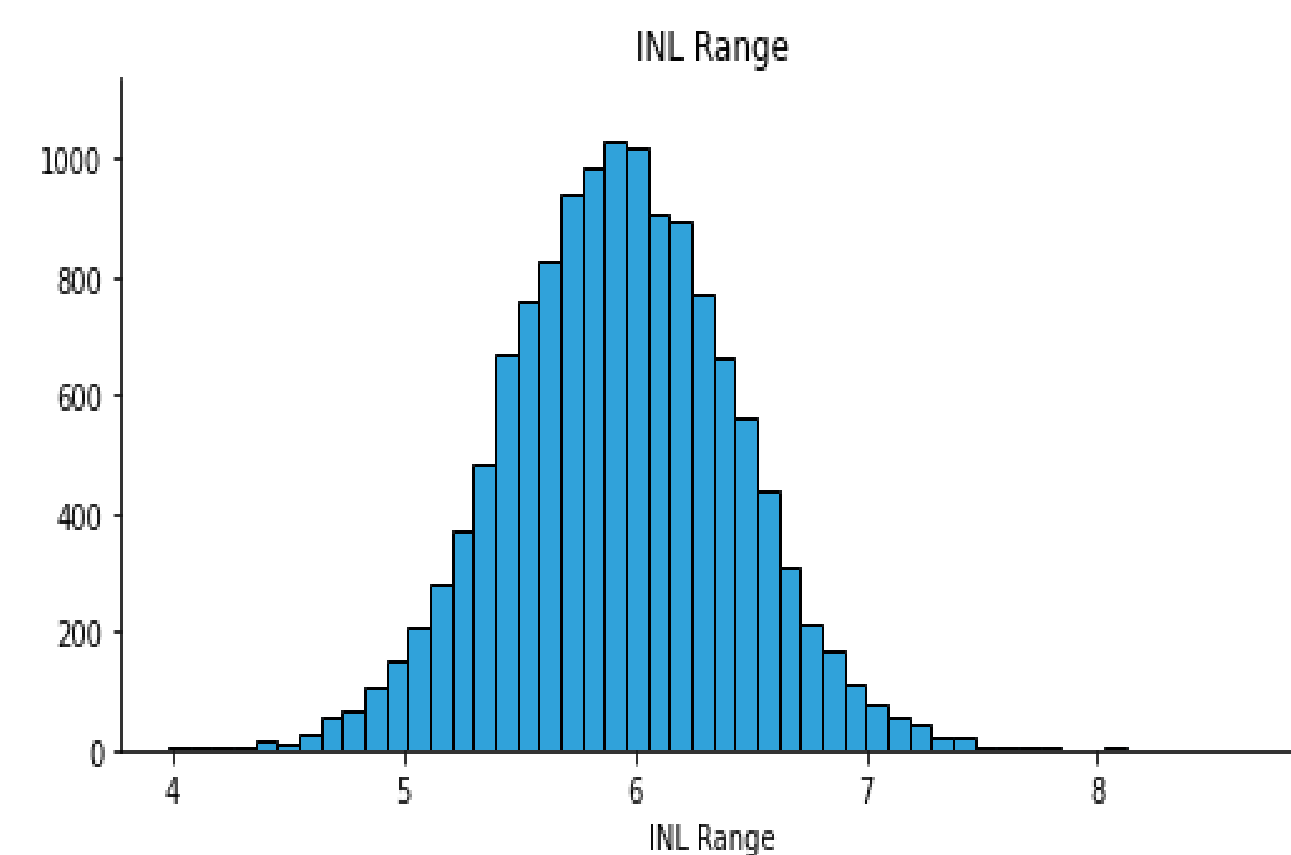


Figure 7 – ADC INL Range Distribution

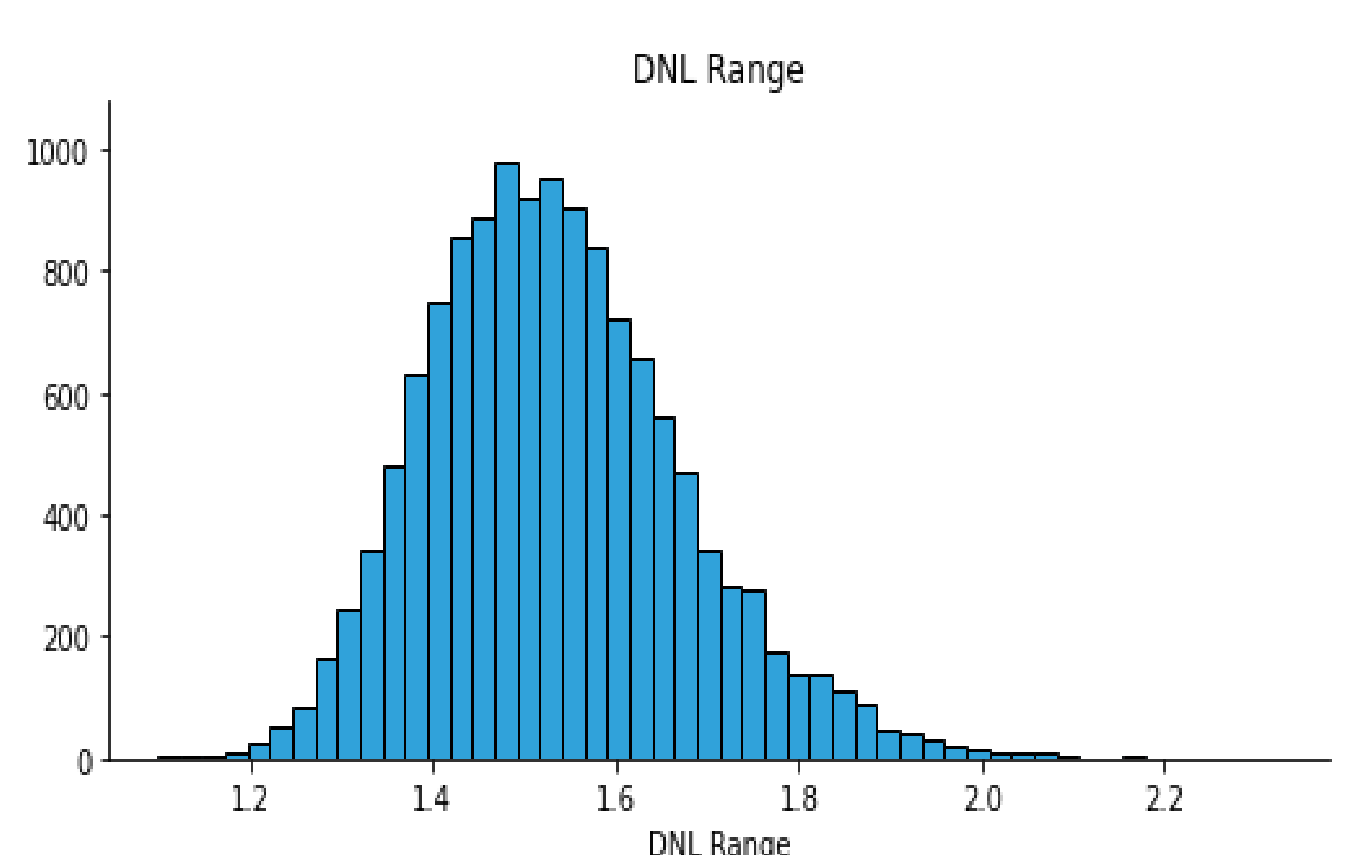


Figure 8 – ADC DNL Range Distribution

The wafer scale sensor has been tested in a JEOL-1400 electron microscope (see figure 8) and a suitable housing (see figure 9).



Figure 9 – Electron microscope set-up



Figure 10 – Quantum C100 vacuum housing

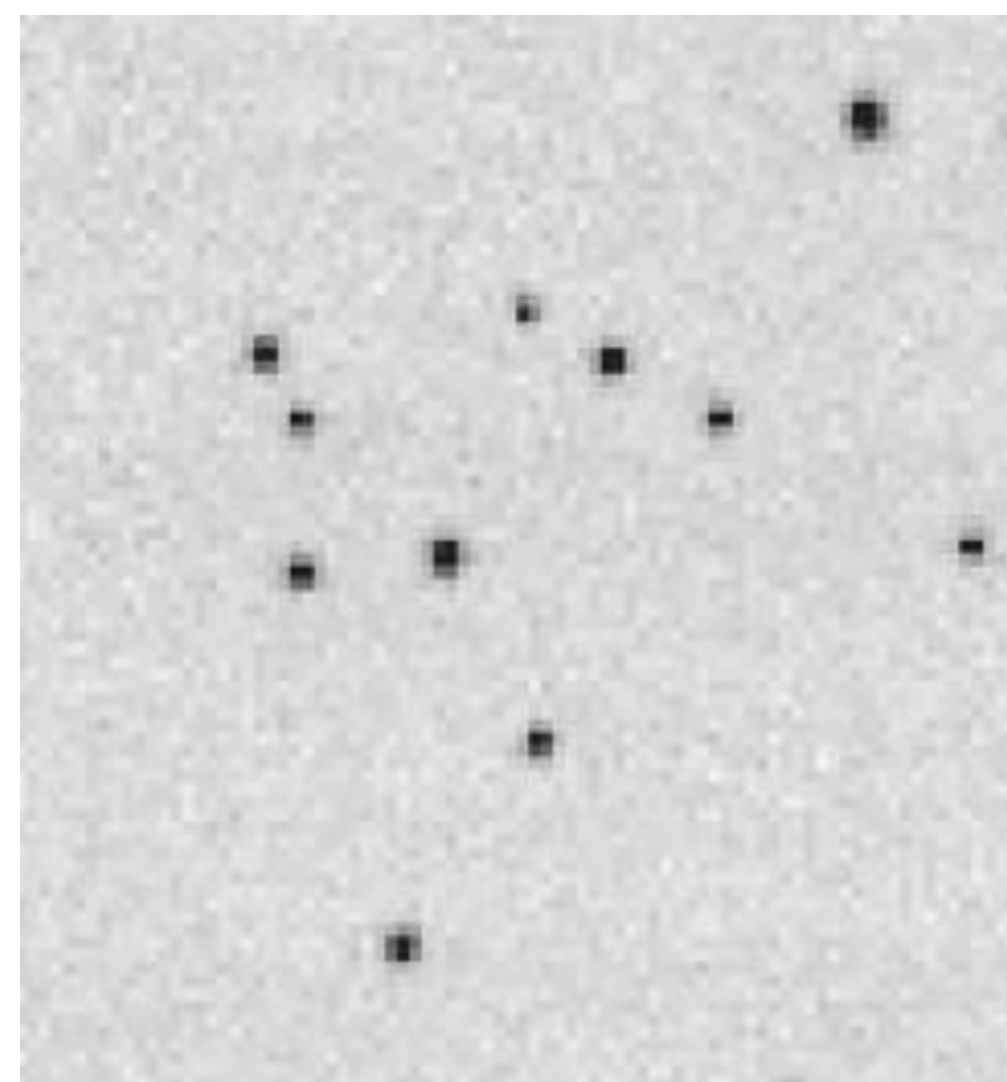


Figure 11 – 100keV electrons single events

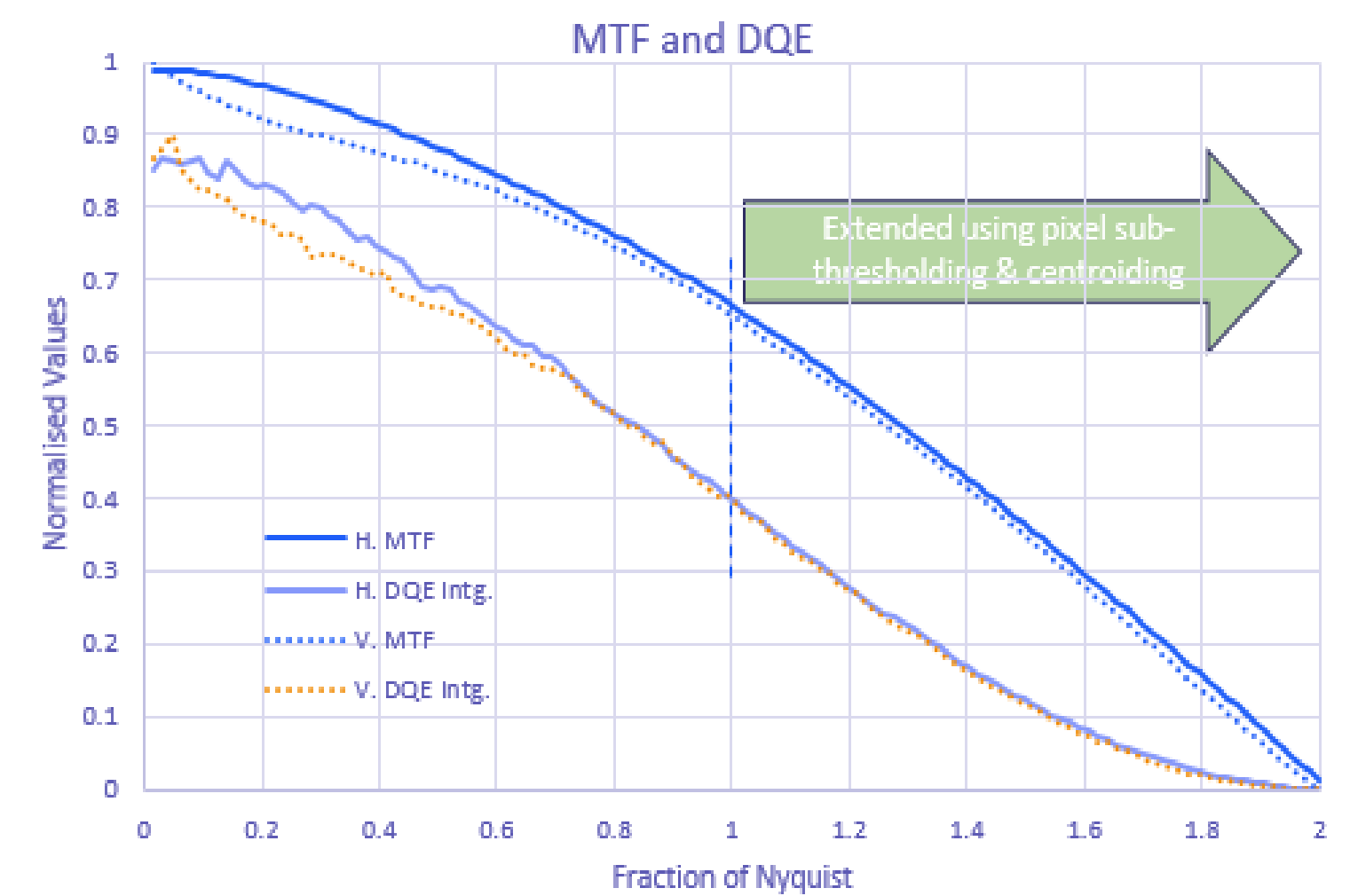


Figure 12 – MTF and DQE



Figure 13 – Rosalind Franklin Picture taken with C100 sensor

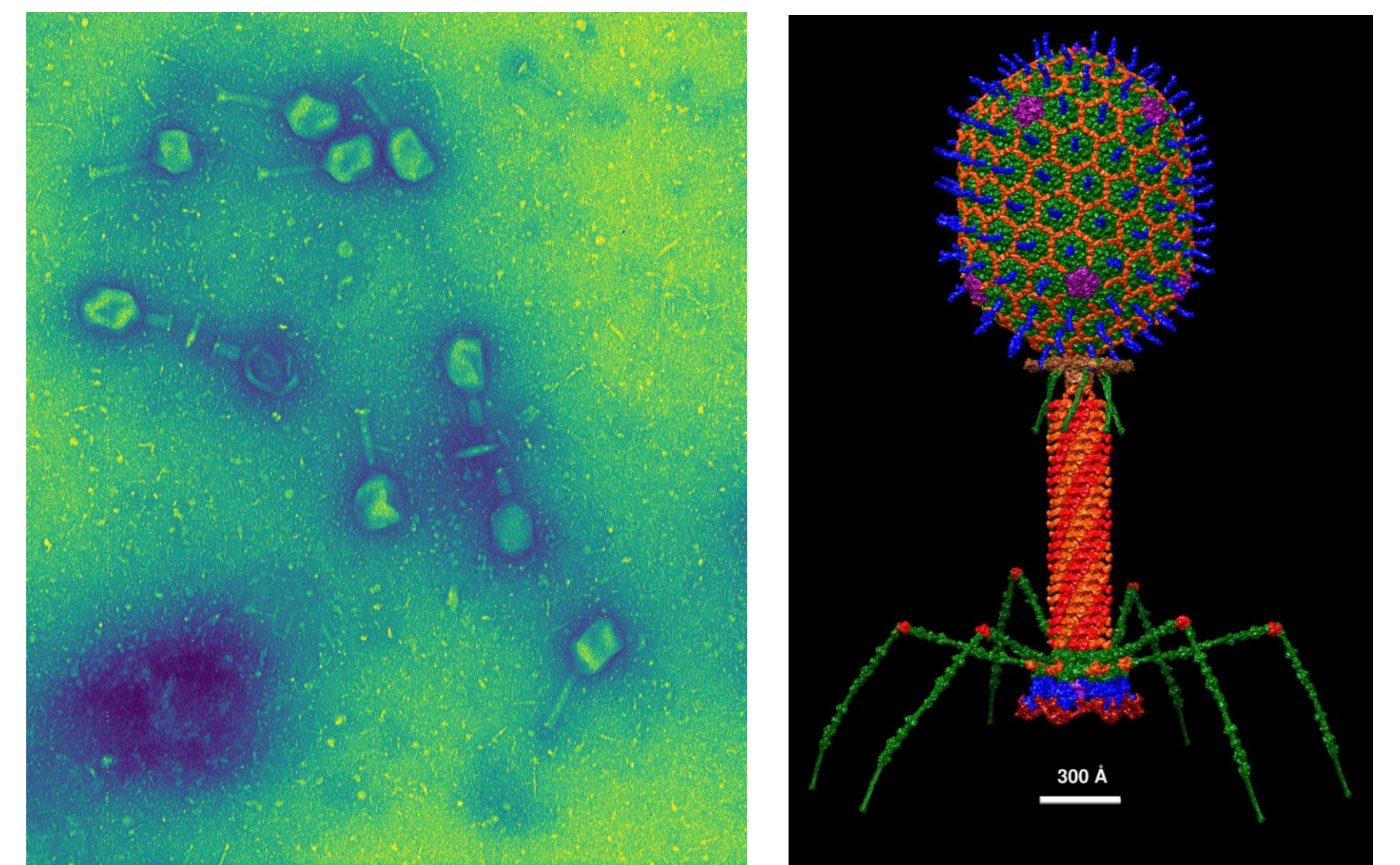


Figure 14 – Image of bacteriophage with C100 using 100keV electrons and its complete structural model ([https://en.wikiversity.org/wiki/WikiJournal\\_of\\_Science/Structural\\_Model\\_of\\_Bacteriophage\\_T4](https://en.wikiversity.org/wiki/WikiJournal_of_Science/Structural_Model_of_Bacteriophage_T4))

## Conclusions

Quantum C100, wafer scale CMOS image sensor, is optimised for cryo-electron microscopy at 100keV. The measured DQE and MTF proves the excellent performance of C100, which will go into production in the second half for 2025.

## References

- (1) M. J. Peet et al., ‘The energy dependence of contrast and damage in electron cryomicroscopy of biological molecules’, Ultramicroscopy 203 (2019) 125–131.
- (2) I Sedgwick et al., ‘LASSENA: A 6.7 megapixel, 3-sides buttable wafer-scale CMOS sensor using a novel grid-addressing architecture’, Proceedings of the International Image Sensors Workshop, 2013
- (3) Heo, Sung Kyn, Kosonen, Jari et al. ‘12-inch-wafer-scale CMOS active-pixel sensor for digital mammography’. Proc SPIE. 7961. 10.1117/12.878053.
- (4) A. Khakoni and G. Gielen, ‘Low-Noise Detectors through Incremental Sigma-Delta ADCs,’ in Analog Electronics for Radiation Detection, Abingdon, CRC Press, 2016, pp. 71-90
- (5) I. Sedgwick et al., ‘PRECISE: A 5Gbps Serialiser for Scientific Detectors in a 180nm CMOS Image Sensor Process’, Proceedings of NSS-MIC 2022, doi: 10.1109/NSS/MIC44845.2022.10399290